IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: Timothy J. Davis et al	)
	)
Application No. (TBA)	) Group Art Unit 2812
Division of Application No. 09/231,083	)
	) Examiner H. Kwok
Filed: Even Date Herewith	)
	)
For: INTEGRATED LARGE AREA	)
MICROSTRUCTURES AND	)
MICROMECHANICAL DEVICES	)
	)

PRELIMINARY AMENDMENT

Honorable Commissioner for Patents
Washington, D.C. 20231

Sir:

Amend the subject application as follows:

IN THE SPECIFICATION:

Page 1, between lines 8 and 9, please insert the following paragraph:

- - This application is a division of U.S. Application No. 09/231,083, filed January 14, 1999, now abandoned. - -

IN THE CLAIMS:

Please add the following claims:

--11. A micromechanical stage comprising:

a released large area platform;

an electromechanical actuator integral with said platform; and

electrical control means for accurately positioning said platform by application of electrostatic potential to said actuator.

--12. The device of claim 11, wherein said actuators are located to enable said stage to be positioned in more than one direction.

--13. The device of claim 11, wherein said control means includes means for positioning with an accuracy of better than 50 nm.

--14. A process for fabricating a micromechanical device comprising:

producing a first pattern on the top surface of a substrate;

etching said pattern to form a first trench in the substrate with a depth of less than twenty (20) percent of the substrate thickness;

producing a second pattern on the bottom surface of the substrate;

etching said second pattern to form a second trench in the substrate with a depth which is less than the thickness of the substrate minus the depth of the trench formed from the top surface;

further etching said top surface trench to cause the bottom of said first trench to intersect with said second trench.

--15. The process of claim 14, wherein said etching is accomplished by reactive ion etching techniques.

--16. The process of claim 14, wherein said substrate is a silicon wafer.

--17. The process of claim 14, wherein the step of etching said pattern to form said first trench includes etching to a depth of between 20 and 50 microns.

--18. A process of fabricating a micromechanical device comprising:

producing a first pattern on the top surface of a substrate;

etching said pattern to form a trench in the substrate with a depth of less than twenty (20) percent of the substrate thickness;

producing a second pattern on the bottom surface of the substrate; and

etching said second pattern to form a trench in the substrate to a depth which causes said trench to intersect with the trench formed by etching from the top surface.

--19. A process for fabricating a micromechanical device comprising;

producing a first pattern on the top surface of a substrate;

etching said pattern to form a plurality of trenches in the substrate with a depth of less than two (20) percent of the substrate thickness;

producing a second pattern on the bottom of the surface of the substrate, said second pattern aligned with the top surface pattern such that at least one structure defined by said second pattern lies directly opposite at least one trench formed from the top surface;

etching said second pattern to form a trench in the substrate with a depth which is less than the thickness of the substrate minus the depth of the

trench formed from the top surface;

further etching said top surface trenches to cause at least one pair of adjacent trenches to overlap and thereby release the structure between them, and to cause the bottom of at least one trench to intersect with the trench previously formed by etching from the bottom surface.

--20. A process for fabricating a solid, large area platform mounted in a cavity in a wafer for motion with respect to the water by integral, flexible supports, comprising:

producing on a top surface of the wafer a first pattern defining the size, shape and location of a large area platform, supports and electrodes for the platform;

etching through said first pattern to produce in a top portion of the wafer top surface trenches surrounding mesas corresponding to said platform, said supports and said electrodes;

depositing a protective layer on said mesas, the walls of said trenches and the bottom surfaces of said trenches;

producing on a bottom surface of the wafer a second pattern corresponding to the size, shape and location of said platform;

etching through said second pattern to produce in a bottom portion of the wafer a bottom trench corresponding to said platform, the bottom trench being aligned with but space below the top trench surrounding the mesa

corresponding to said platform;

removing the protective layer from the bottom surfaces of the top trenches; and

further etching the top trenches to cause the top surface trench surround the mesa corresponding to said platform to intersect said bottom trench to produce a through trench to free said platform, and to undercut said mesas to release said supports and said electrodes from the wafer underlying the supports and electrodes, the ends of said supports being integral with and cantilevered from the wafer and the platform and extending therebetween to support the platform.

--21. The process of claim 20, wherein producing said first and second pattern includes coating the wafer with an oxide layer and producing said pattern in said oxide layer by photolithography and etching.

--22. The process of claim 20, wherein said etching of trenches includes performing silicon etching by reactive ion etching techniques.

--23. The process of claim 20, further including depositing electrically conductive material on the top surfaces of said platform, said supports and said electrodes.--

REMARKS

The foregoing claims have been added to provide the scope of protection to which applicants are believed entitled.

In the event that the restriction requirement in the parent application is repeated, applicants hereby elect process claims 1-10 and 14-23, without traverse.

Respectfully submitted,
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